

# Clock Management Time (CMT) Test Results

Analyzed by Kevin Wray, Boeing

## I. Introduction

The Clock Management Tiles (CMTs) in Xilinx 7 Series devices consist of one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL). The CMTs are organized as vertical columns adjacent to the I/Os, and provide access to vertical global clock routes and horizontal regional clock routes, as shown in Figures 1 and 2. The 7VX980TRF1930ABX1637 device tested contains a total of 18 CMTs. The basic features of both the MMCM and PLL primitives are frequency synthesis, phase shift and de-skew, and jitter filtering. The PLL contains a subset of the advanced MMCM features. Some differences in SEE test results are to be expected due to the differences in programmability as well as fundamental implementation- analog PLLs and digital MMCMs. Complete details of the CMT functions and clock routing resources are documented in the 7 Series FPGAs Clocking Resources User Guide, UG472.

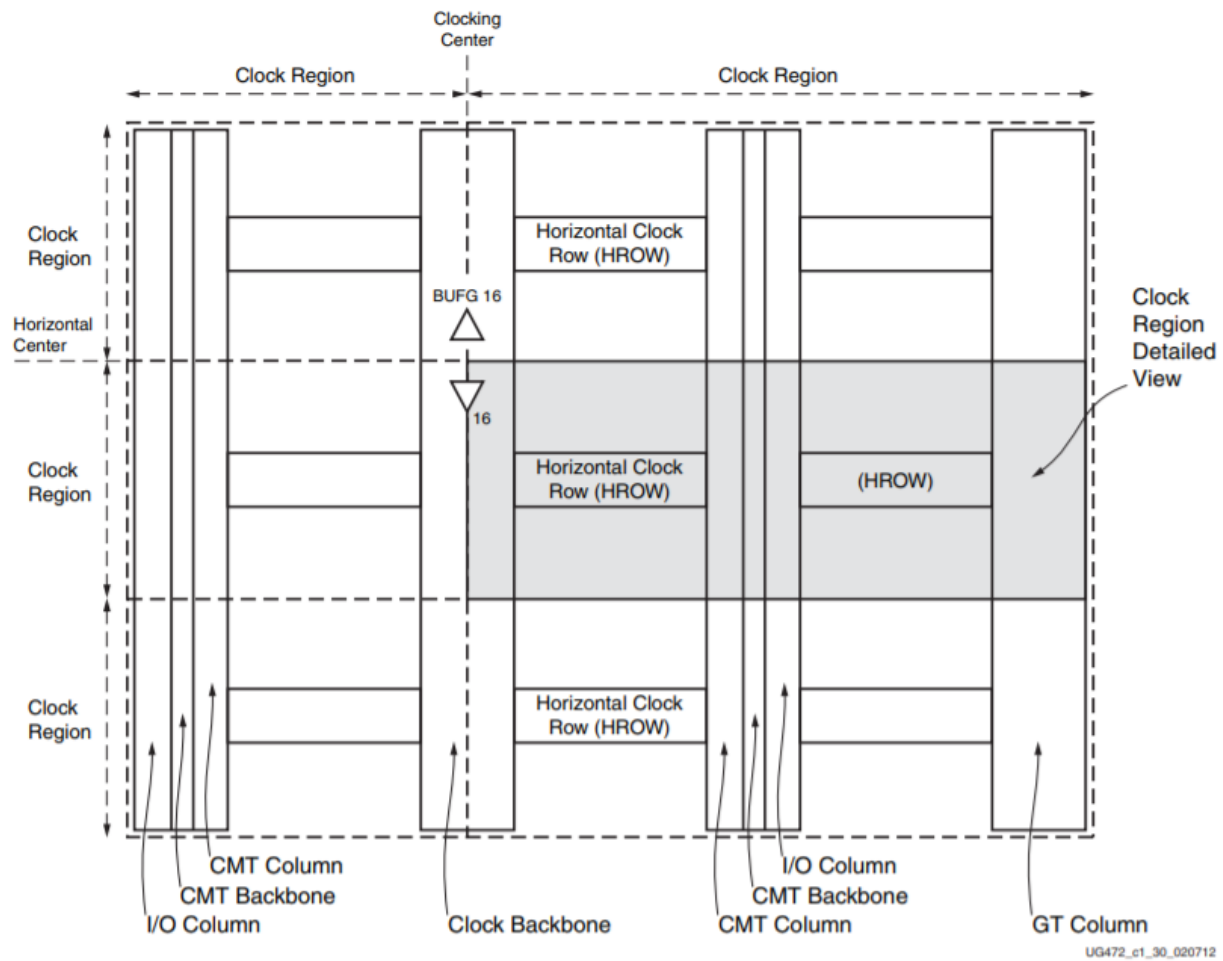


Figure 1: 7 Series FPGA High-Level Clock Architecture View

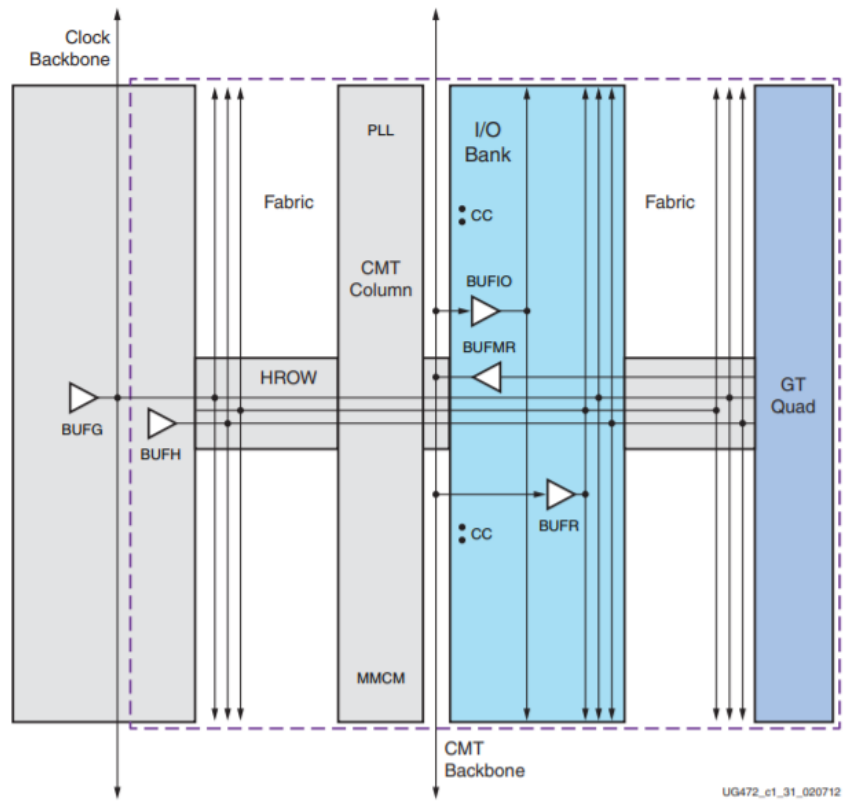


Figure 2: Basic View of 7 Series Clock Region

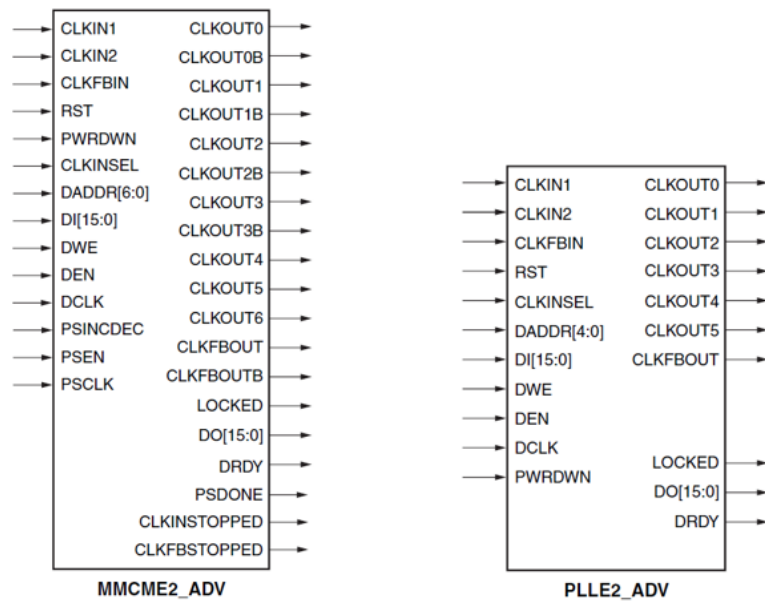


Figure 3: MMCM and PLL Device Primitives

## II. Test Methodology and IP

The Virtex-7 SEE clocking test was leveraged from the V5QV heritage DUT design, originally conceived and implemented by George Madias of Boeing. A basic block diagram of the DUT test design is shown in Figure 4. The test module consists of dual redundant clocks that are independently monitored for upsets. The input clocks are frequency multiplied 2x by the MMCM/PLLs, and the outputs are checked via validation circuitry implemented a triple-modular redundancy (TMR) configuration. The overall DUT design contains two copies of this test instance.

Each test instance contains a primary and secondary clocking source (MMCM or PLL). If the primary is upset, the validation circuit will switch to the secondary while resetting the upset source. If the secondary was affected by the same event, then the validation circuit will switch again and reset the secondary as well. For a really long transient, switching and resetting the clock sources may occur multiple times. This upset mitigation scheme produces three distinct error signatures observed by the FuncMon:

- *single clock upset* – a brief outage (<100 ms) on the primary clock, resolved by the validation circuit successfully switching to the secondary source
- *instance outage* – longer outages (>100 ms) effecting both the primary and secondary clock of a test instance, where the validation circuit is not immediately effective but eventually correct operation resumes
- *global outage* – longer outages (>100 ms) effecting both clocks of both test instances simultaneously, resolved by either the validation circuit eventually or via external reset from Funcmon

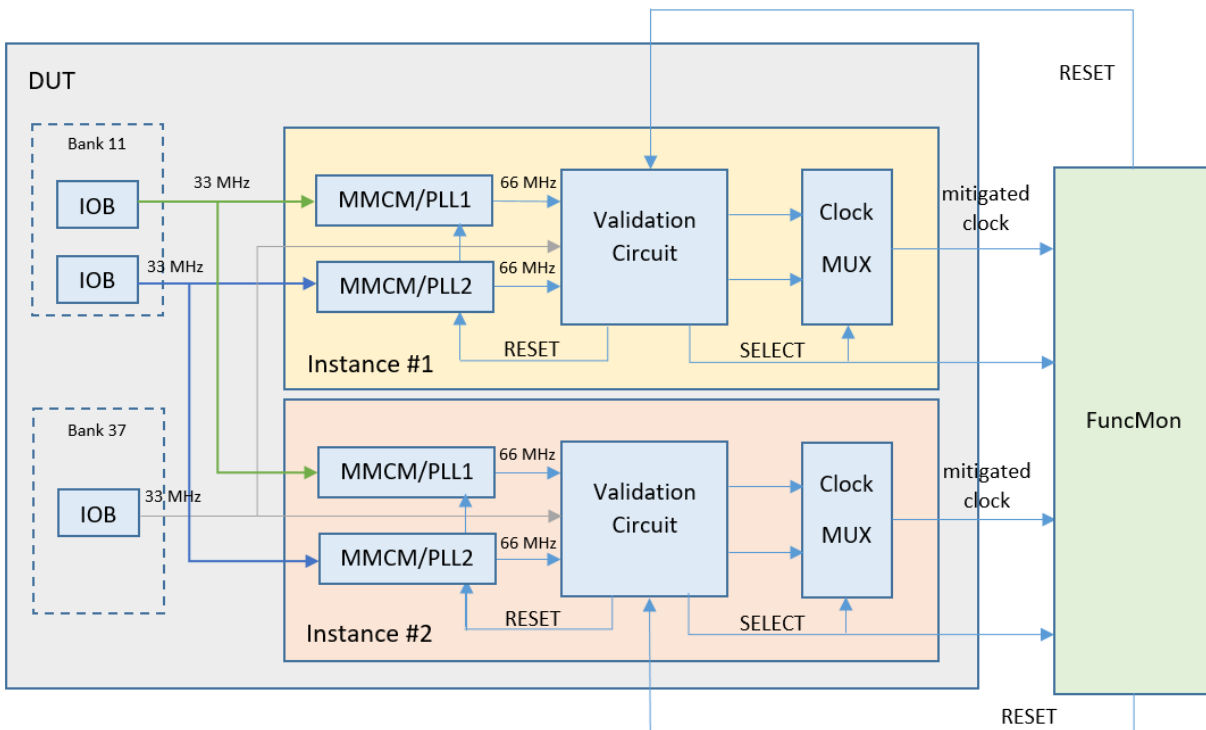


Figure 4: 7 Series CMT DUT Design Block Diagram

The FuncMon system for both clock tests was identical as are the DUT designs with, of course, the exception of the clock source instantiated. Additionally, the FuncMon observes the mitigated clock output from each instance. When a clock output from either instance stops for 10 seconds, FuncMon and the validation circuit are externally reset, and FuncMon records a global outage event. After X seconds enough time has passed for events caused by a configuration upset to be scrubbed out as ConfigMon accomplishes a readback and scrub cycle in less than one second. Therefore external intervention is required to reset the DUT. It is important to note that no SEFI-like events were seen in this testing; that is there were no clock outages that could not be reset; thus, reconfiguration was never needed to recover an upset clock source.

### III. Results: Measured Cross Sections

The MMCM and PLL cross sections for the three different error signatures are shown in Figures 5 and 6, respectively, measured as a function of LET.

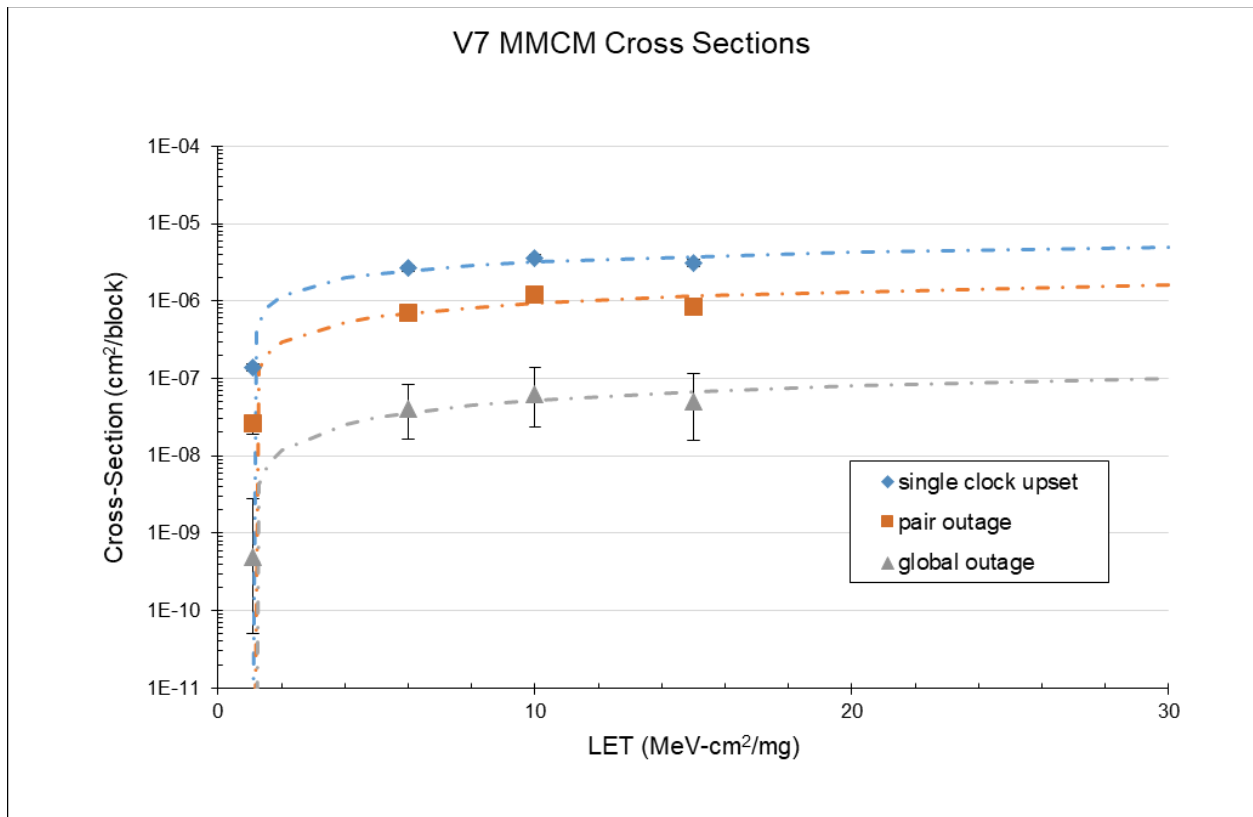


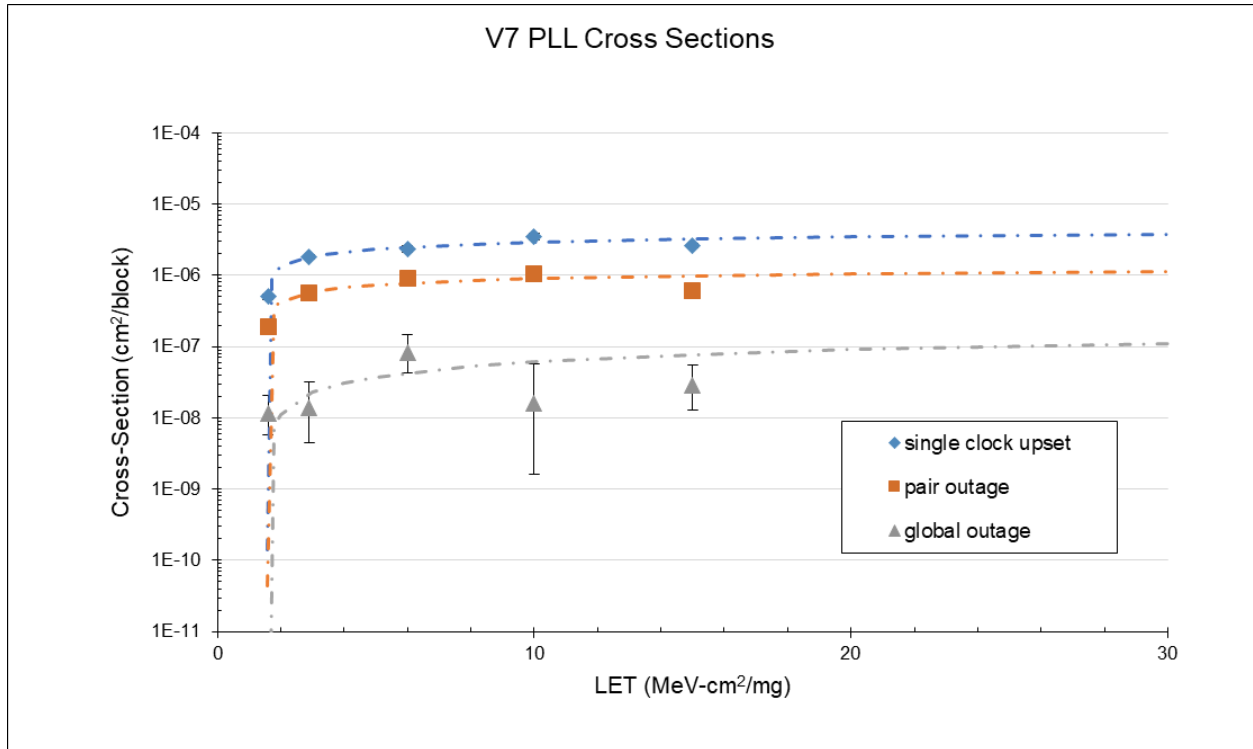
Figure 5: Virtex-7MMCM Heavy Ion Cross-sections

Weibull fit parameters:

(a) Single:  $\sigma_{sat} = 1 \times 10^{-5}$ ,  $L_{th} = 1.09$ ,  $W = 65.0$ ,  $S = 0.49$

(b) Instance:  $\sigma_{sat} = 4 \times 10^{-6}$ ,  $L_{th} = 1.09$ ,  $W = 99.7$ ,  $S = 0.55$

(c) Global:  $\sigma_{sat} = 2 \times 10^{-7}$ ,  $L_{th} = 1.09$ ,  $W = 48.0$ ,  $S = 0.71$



**Figure 6: Virtex-7 PLL Heavy Ion Cross-sections**

**Weibull fit parameters:**

**(a) Single:**  $\sigma_{sat} = 8 \times 10^{-6}$ ,  $L_{th} = 1.59$ ,  $W = 129.0$ ,  $S = 0.29$

**(b) Instance:**  $\sigma_{sat} = 2 \times 10^{-6}$ ,  $L_{th} = 1.59$ ,  $W = 49.8$ ,  $S = 0.30$

**(c) Global:**  $\sigma_{sat} = 3 \times 10^{-7}$ ,  $L_{th} = 1.59$ ,  $W = 104.7$ ,  $S = 0.59$

To some extent, error signatures and their causes can be correlated. An instance outage is the result of hitting something common to both the primary and secondary clock sources, whereas a global outage is the result of hitting something common to all clock sources under test. From the block diagram in Figure 4, we see there are three external clocks coming into the DUT. One input provides the first clock source to each test instance, and another provides the redundant source. The third clock is used for the validation and control circuitry. Since the clock sources under test for both instances came from the same I/O bank, an upset to that I/O bank would cause a clock global outage observed by the validation circuitry. A single IOB hit on the other hand, would manifest in a single clock upset observed by both test instances.

We can compare the computed CMT cross sections to that of the IOBs in Section x to derive some assumptions. On average, the cross section for an individual LVCMOS18 or LVDS IOB upset is 2-3 orders of magnitude lower than those computed for the MMCM/PLL single clock upset or instance outage categories. Therefore the I/O circuitry has minimal effect on clocking upsets in these two categories, and reported cross sections are representative of the MMCM/PLL blocks, clock routing, and configuration bits associated with the clocking structure. Weibull fits for MMCM/PLL global upsets and I/O bank upsets are very similar on the other hand, and hence we can assume the majority of global upsets

observed with this clocking design are due to I/O bank hits. Therefore it is likely the true cross-section representing global clocking events is much lower than that reported in Figures 5 and 6.

Table 1 shows GEO-orbit upset rates computed with CREME96 code, for each resource and associated error signature, expressed in units of events/day per resource (MMCM or PLL) instance.

**Table 1: GEO-Orbit Upset Rates**

Signature	Nominal	Worst-Case
MMCM <i>Single</i>	$1.75 \times 10^{-4}$	$1.89 \times 10^{-4}$
MMCM <i>Instance</i>	$4.53 \times 10^{-5}$	$4.95 \times 10^{-4}$
MMCM <i>Global</i>	$3.71 \times 10^{-6}$	$4.11 \times 10^{-6}$
PLL <i>Single</i>	$1.51 \times 10^{-4}$	$1.65 \times 10^{-4}$
PLL <i>Instance</i>	$4.63 \times 10^{-5}$	$5.06 \times 10^{-5}$
PLL <i>Global</i>	$1.86 \times 10^{-6}$	$2.13 \times 10^{-6}$

Similar to the V5QV testing, the measured cross sections and resultant GEO rates for the two different Virtex-7 clock resources were very similar. Figures 7, 8, & 9 below show MMCM and PLL results superimposed for the three different error signatures:

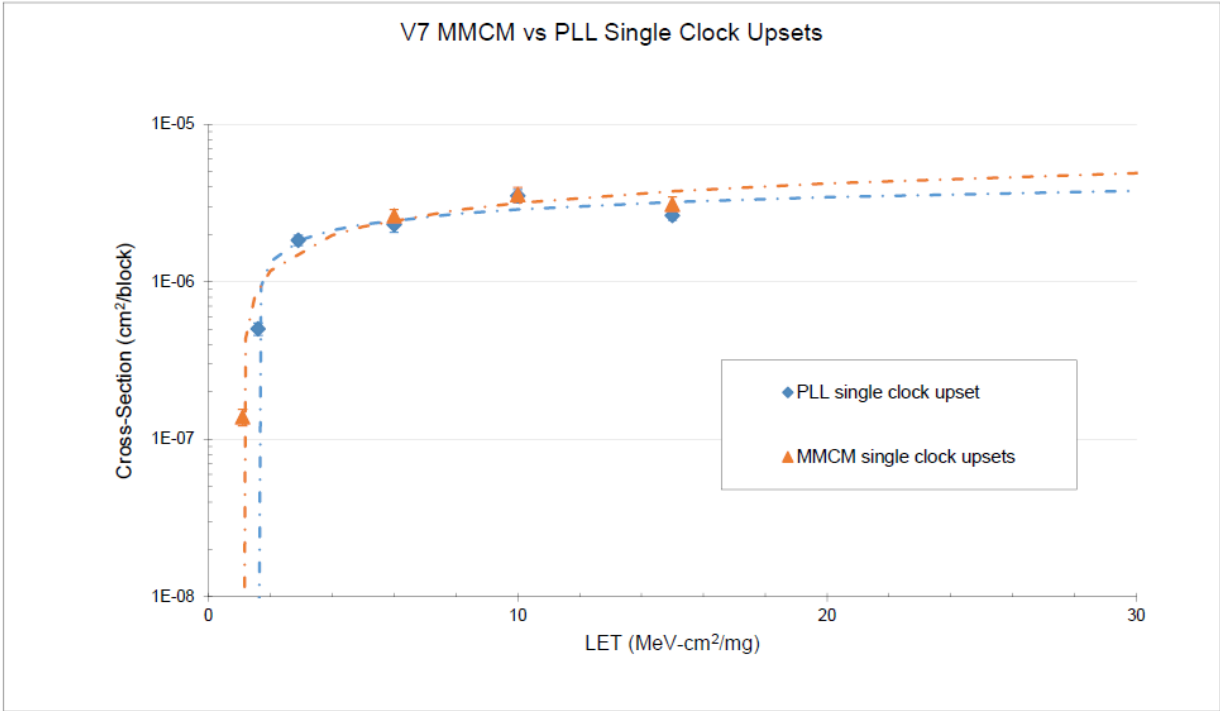


Figure 7: Virtex-7 PLL vs MMCM Single Clock Upsets

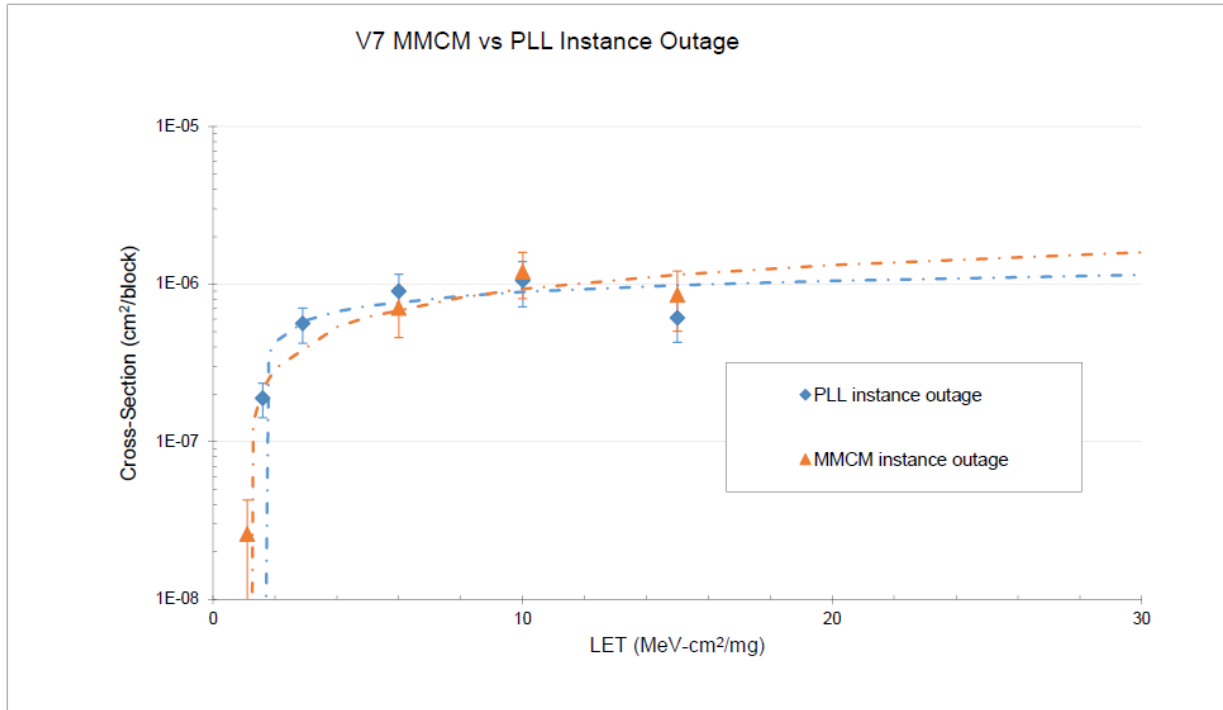


Figure 8: Virtex-7 PLL vs MMCM Instance Outages

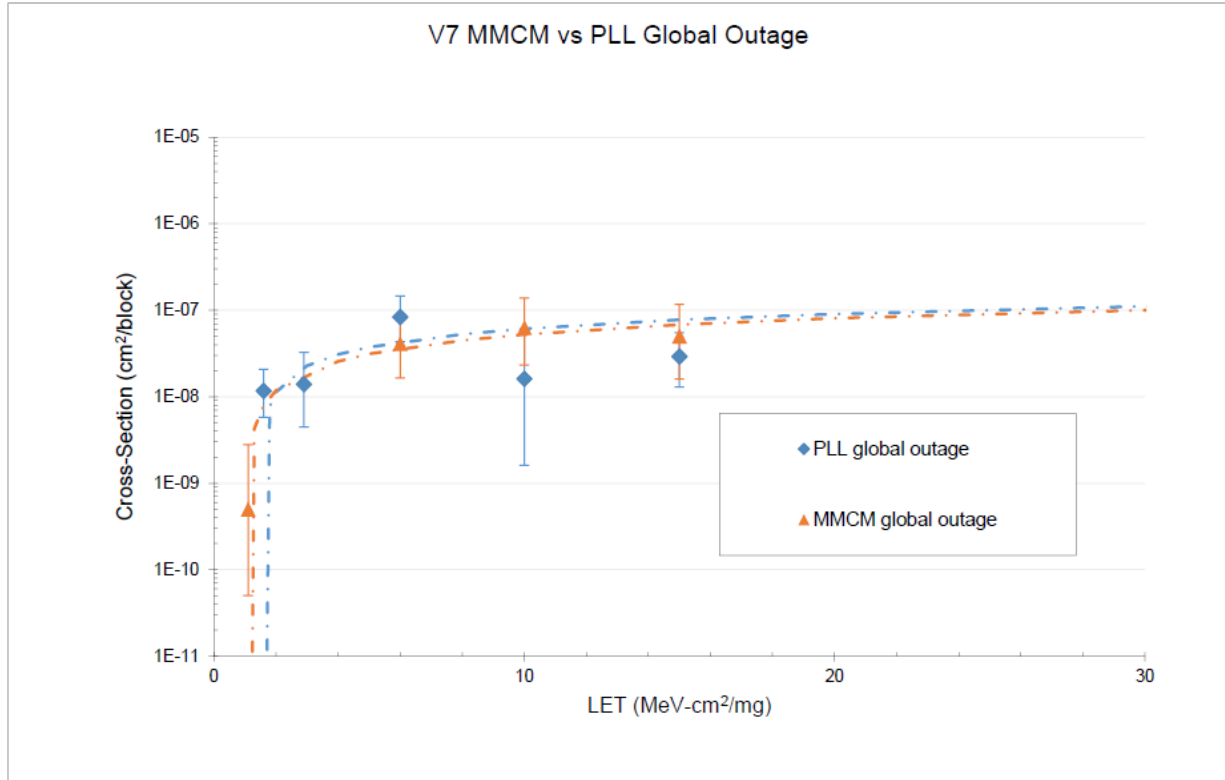


Figure 9: Virtex-7 PLL vs MMCM Global Outages

#### IV. Comparison to V5QV

The data analysis performed for the Xilinx Virtex-7 XRTC SEE test campaign has unveiled problems and inconsistencies in the Virtex-5QV clocking data originally reported in the Architectural Features SEU Characterization Summary. Philosophically, we would expect single clock upsets to occur most frequently, followed next by instance outages, and lastly by global outages being the least frequent. We found this prediction to be true in the Virtex-7 analysis reported here. However, upon comparing the V7 results to V5QV, it was observed that the V5QV cross sections reported for the different error signatures are the reverse of our hypothesis: global hits had the largest cross section and single clock upsets had the smallest. Our conclusion is that the V5QV results presented in the Architectural Features report are flawed.

Taking the raw V5QV data and reanalyzing it using the Virtex-7 Python methodology produced results more in line with our expectations. An errata showing the new V5QV results using the V7 algorithm has been published to the Xilinx Space Lounge. The original V5 data analysis was not revisited to thoroughly identify the source of the errors in the Architectural Features report. Instead, running both raw data sets through the new analysis script provides the most accurate comparison, which is presented here.

A comparison of the Virtex-5QV and Virtex-7 single clock upsets is shown in Figure 10.



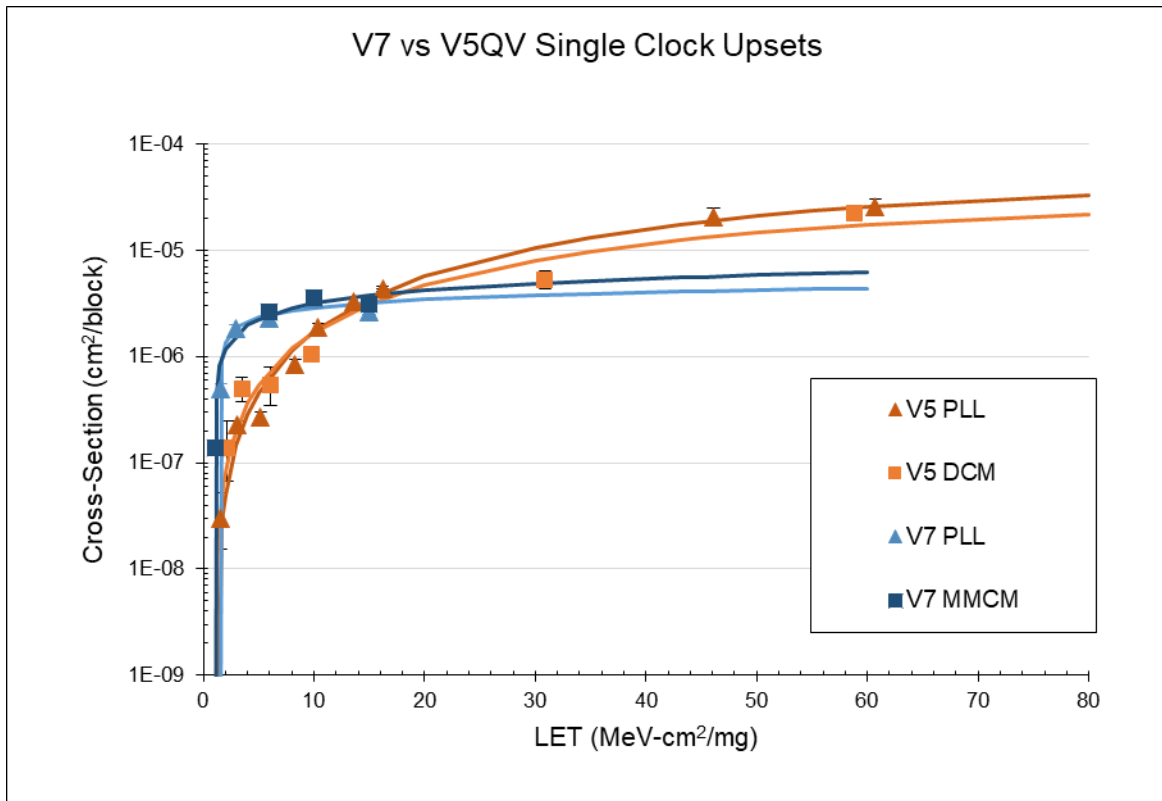


Figure 10: Virtex-7 vs. V5QV Single Clock Upsets

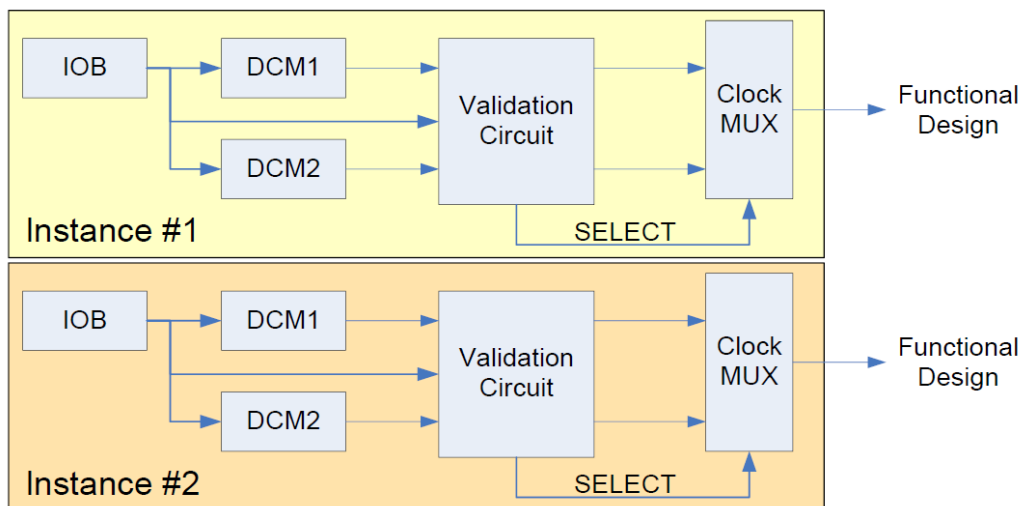


Figure 11: V5QV CMT DUT Design Block Diagram

There is an important difference in the selection of I/O pins used for the clock inputs between the Virtex-7 and Virtex-5QV that has impact on the instance and global outage results. In the original Virtex-5QV design, clock sources from separate I/O banks were used for each test instance as shown in Figure

11 above. In Virtex-7 however, clock sources from the same bank were used for both instances. Therefore an I/O bank hit would manifest in an instance outage in the Virtex-5QV DUT and a global outage in the Virtex-7 DUT. Therefore a more accurate comparison would be Virtex-5QV instance outages to Virtex-7 global outages. This comparison is shown in Figure 12 below, which has a similar shape to the single clock upset comparison.

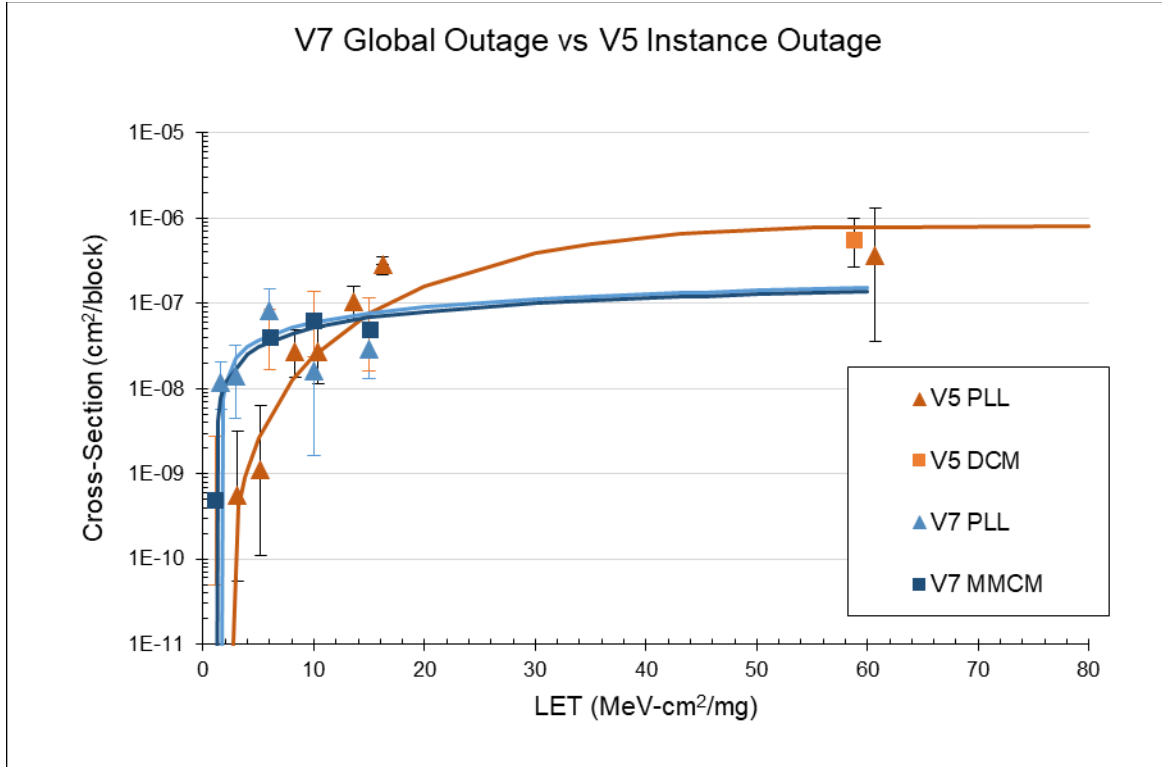


Figure 12: Virtex-7 vs. V5QV Instance Outages

Only a single DCM instance outage was observed using the updated Python analysis, therefore we are unable to obtain a Weibull fit. The single data point for DCM matches PLL curve. The updated Python analysis did not find any Global Outages in the V5QV data.

## V. Summary

The V5QV CMT DUT design was migrated to Virtex-7 technology and used to gather valuable single event effect data on the 7 Series PLL and MMCM blocks. The clock input connections were modified from the original design, and hence leads to some differences in the interpretation of the results between V5QV and Virtex-7. The V5QV clocking scheme is preferred, and is recommended for future testing. Further improvements to the original test methodology are being explored for the KU060 test campaign in order to provide better visibility. Note that the susceptibility of the clock tree distribution is not included. The analysis presented here provides accurate cross section data on the Virtex-7 Clocking Management Tiles that can be used to predict realistic orbit rates and error signatures.